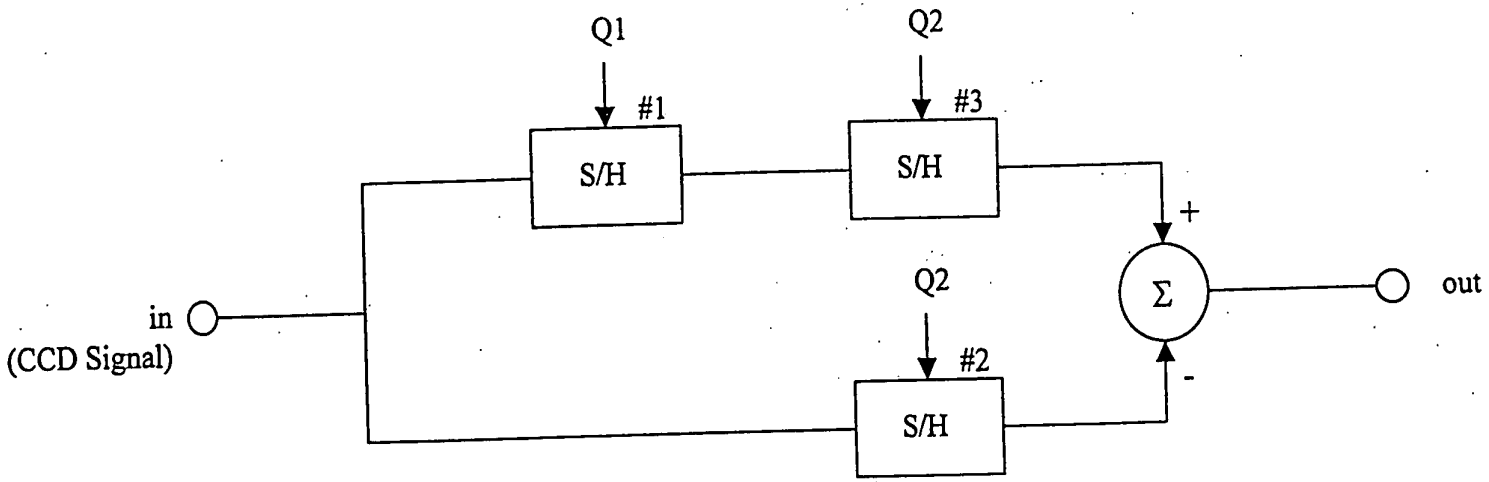

Figure 1: Pipeline CDS Circuit (Prior Art)

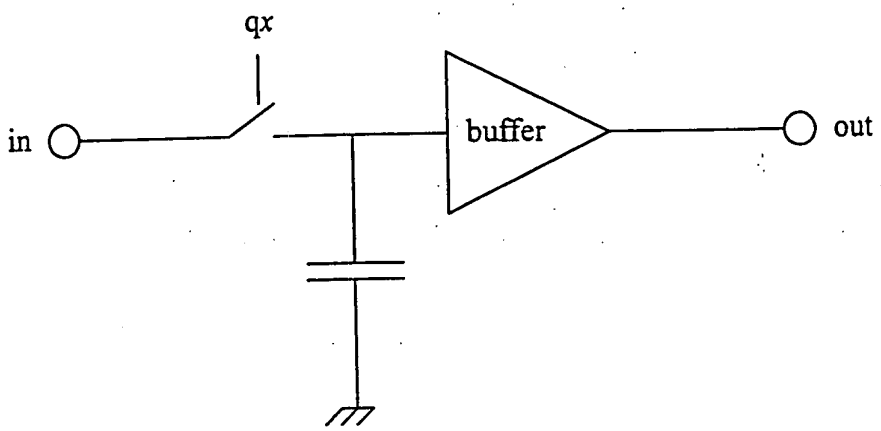

Figure 2: Sample-and-Hold (S/H) Circuit (Prior Art)

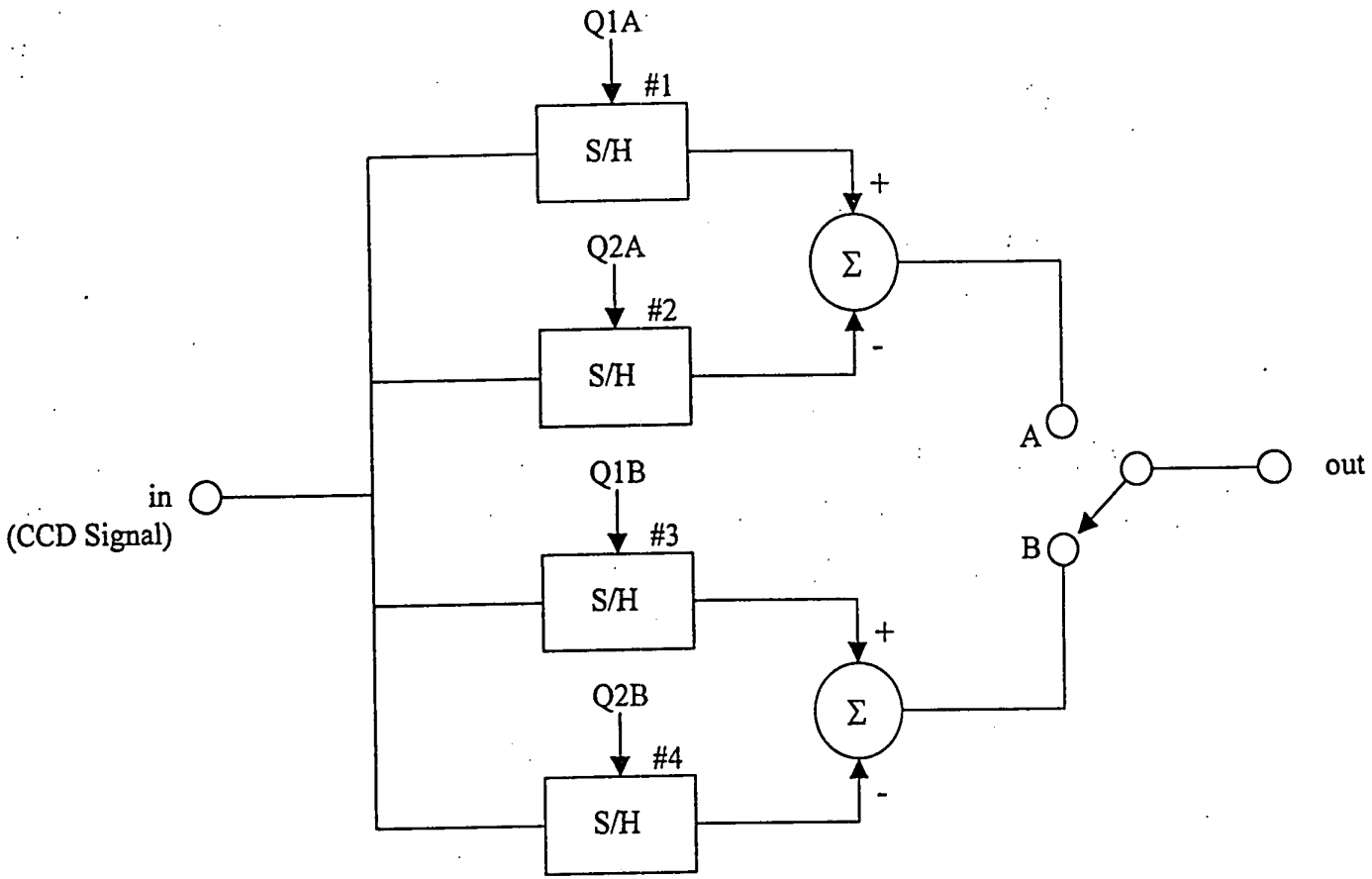

Figure 3: Dual CDS Circuit (Prior Art)

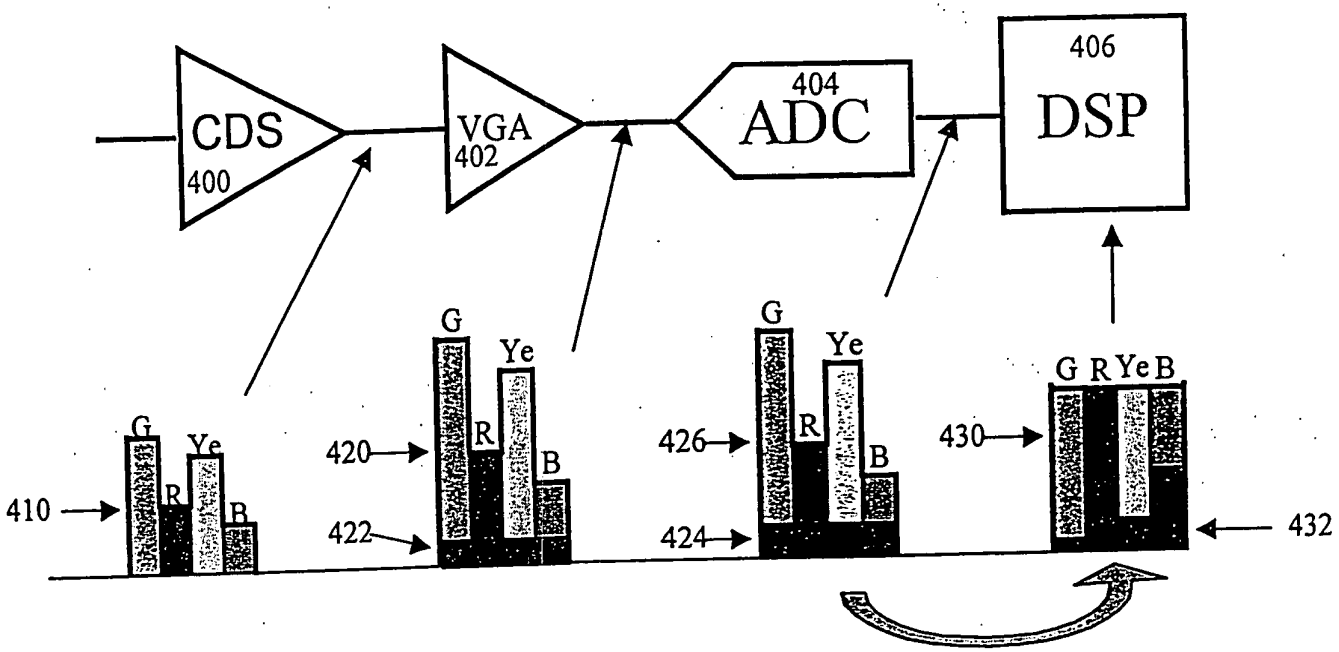

Figure 4: CCD Signal Processing Channel (Prior Art)

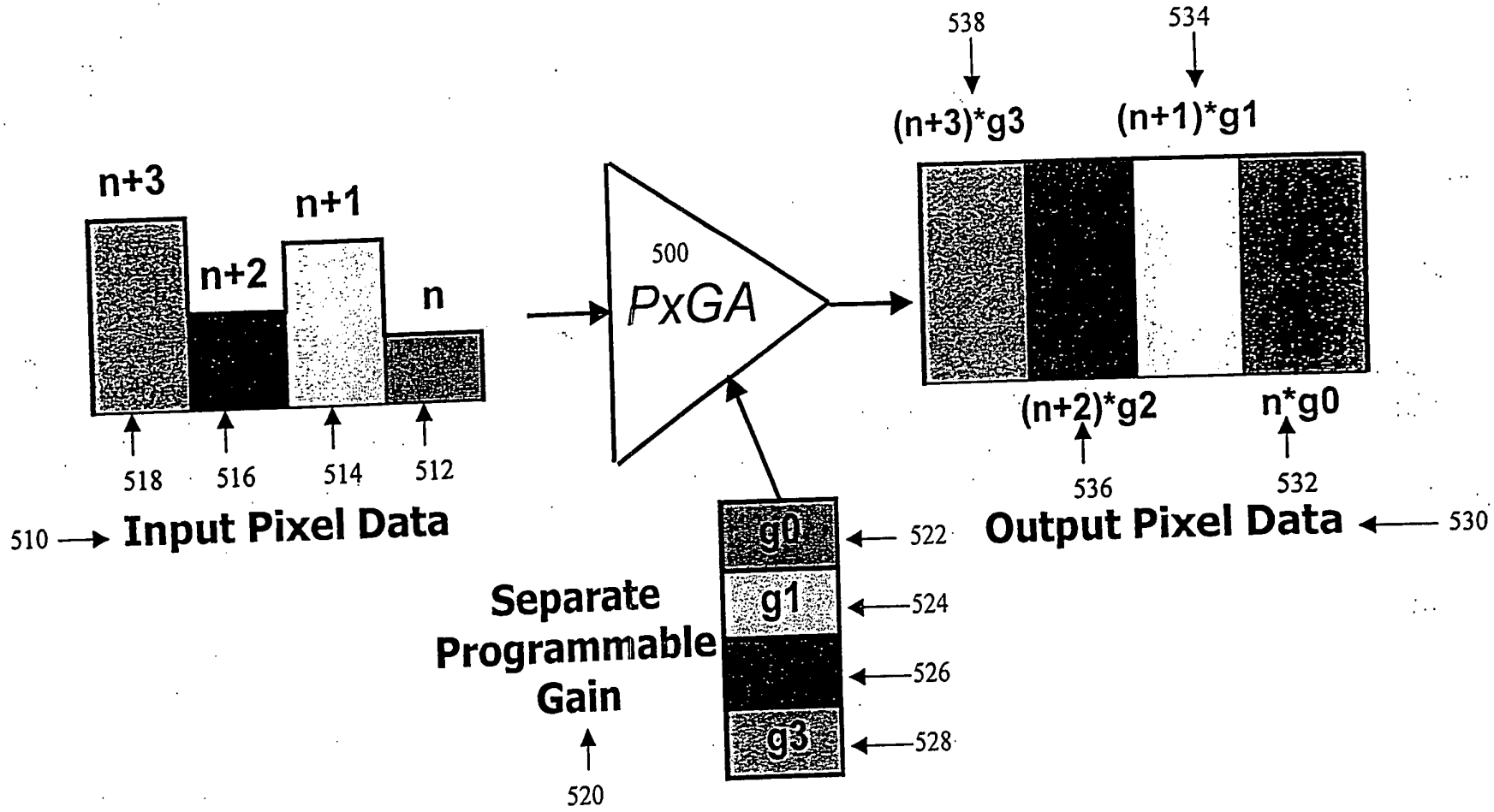

Figure 5: Pixel Gain Amplifier (PxGA)

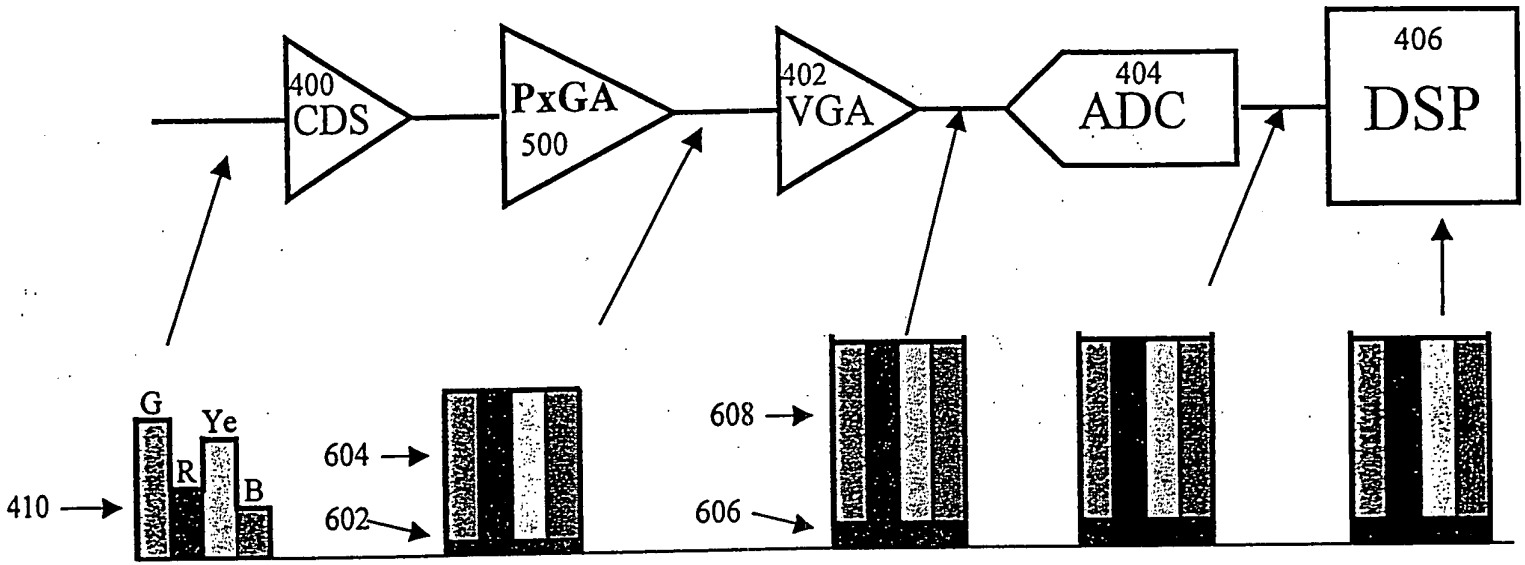

Figure 6: CCD Signal Processing Channel with PxGA

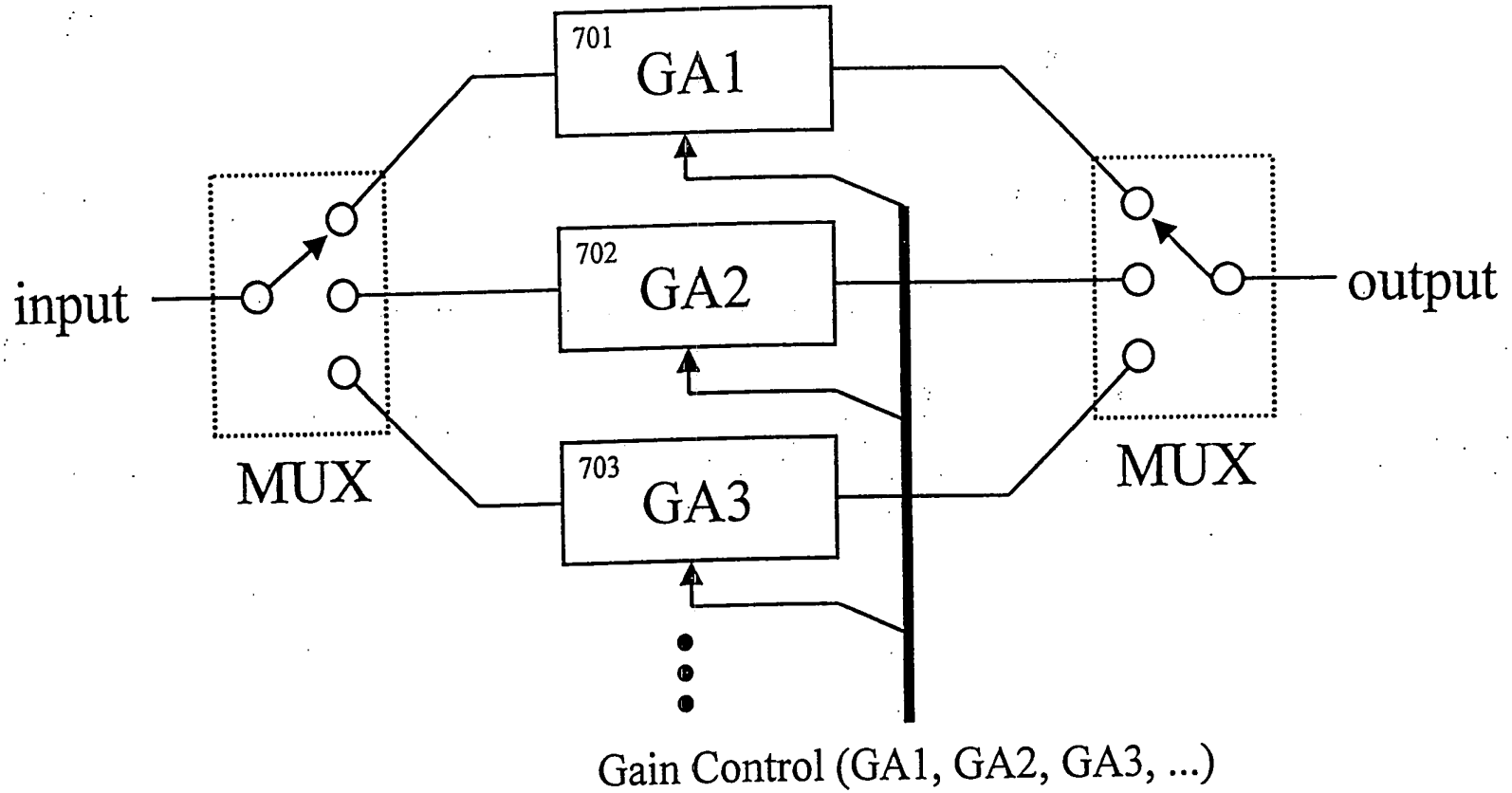

Figure 7: Multiplexed Gain Amplifier (Prior Art)

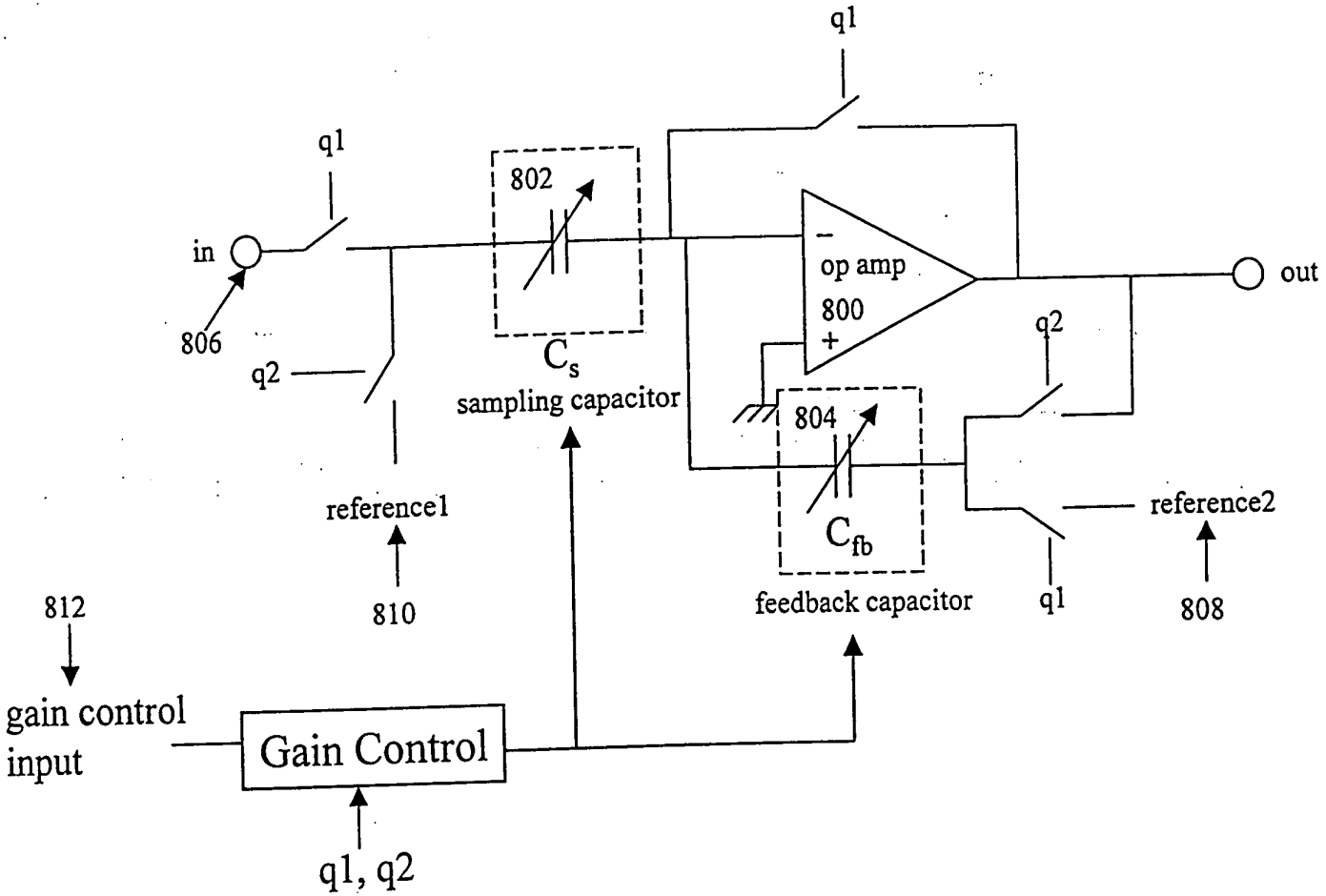

Figure 8(a): PxGA schematic

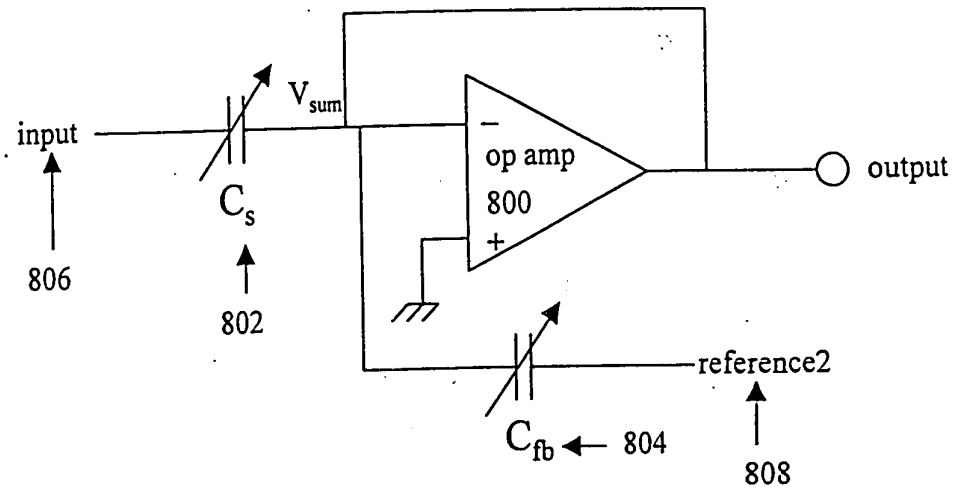

Figure 8(b): PxGA in q1 phase

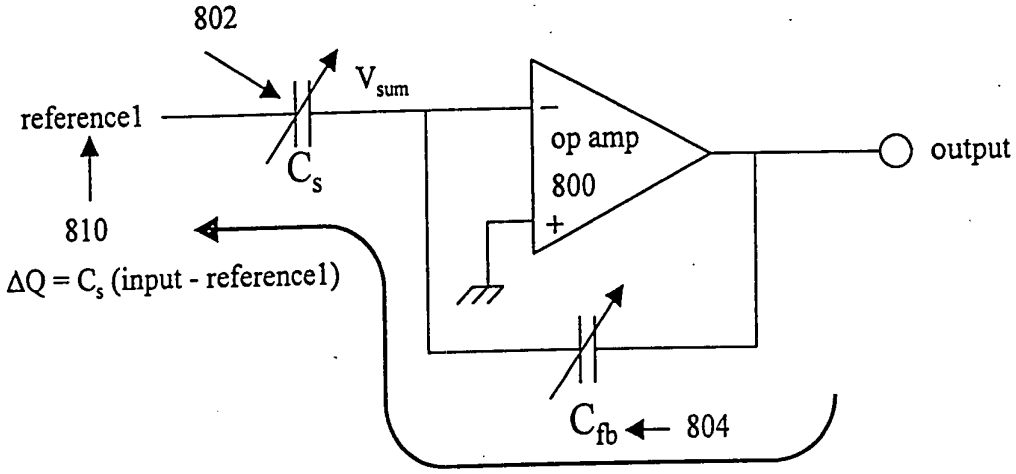

Figure 8(c): PxGA in q2 phase

$$Out = \frac{C_s}{C_{fb}}\left(in_2 - \left(\frac{C_s}{C_{fb}}(in_1 - ref)\right)\right)$$
$$= \frac{C_s}{C_{fb}}\left(in_2 - \frac{C_s}{C_{fb}} in_1 + \frac{C_s}{C_{fb}} ref\right)$$

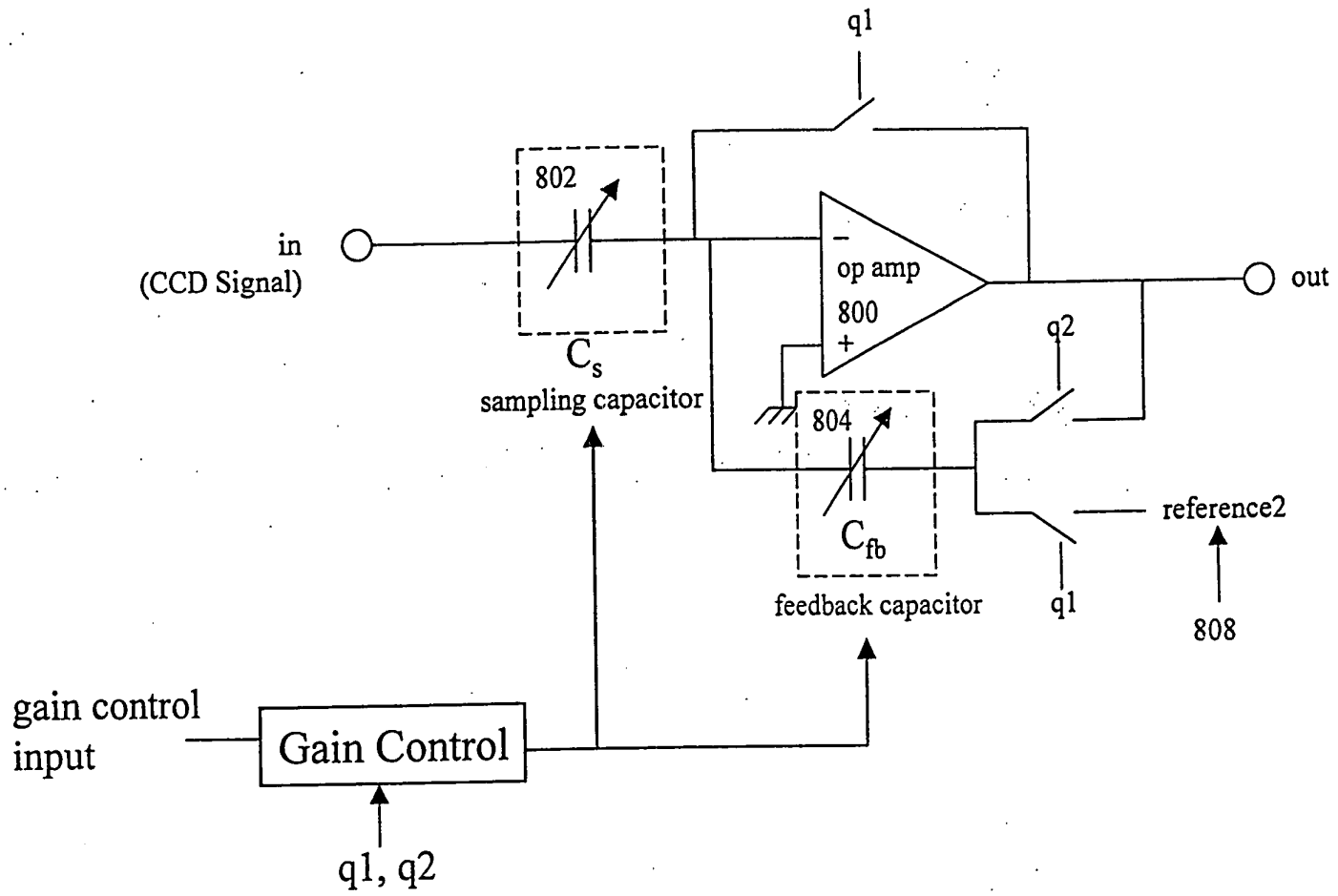

Figure 9: CDS/PxGA schematic

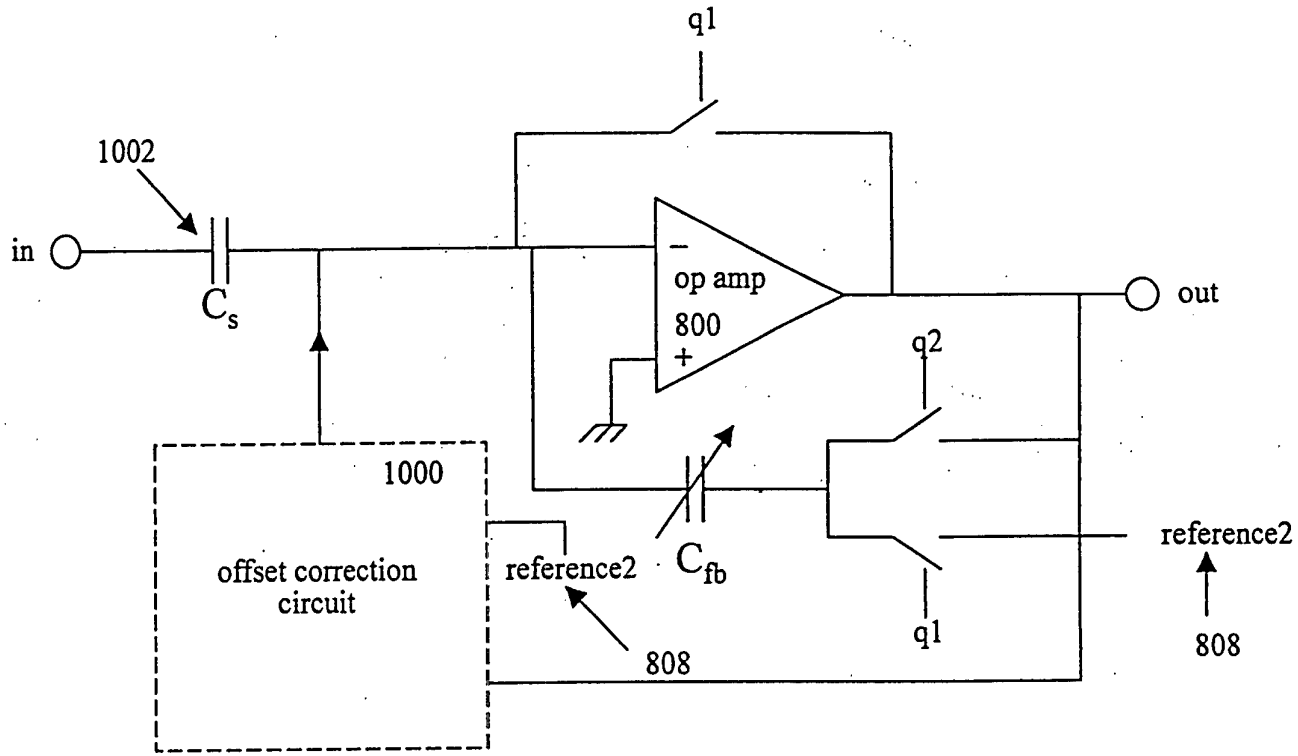

Figure 10: CDS/PxGA Circuit With Offset Correction

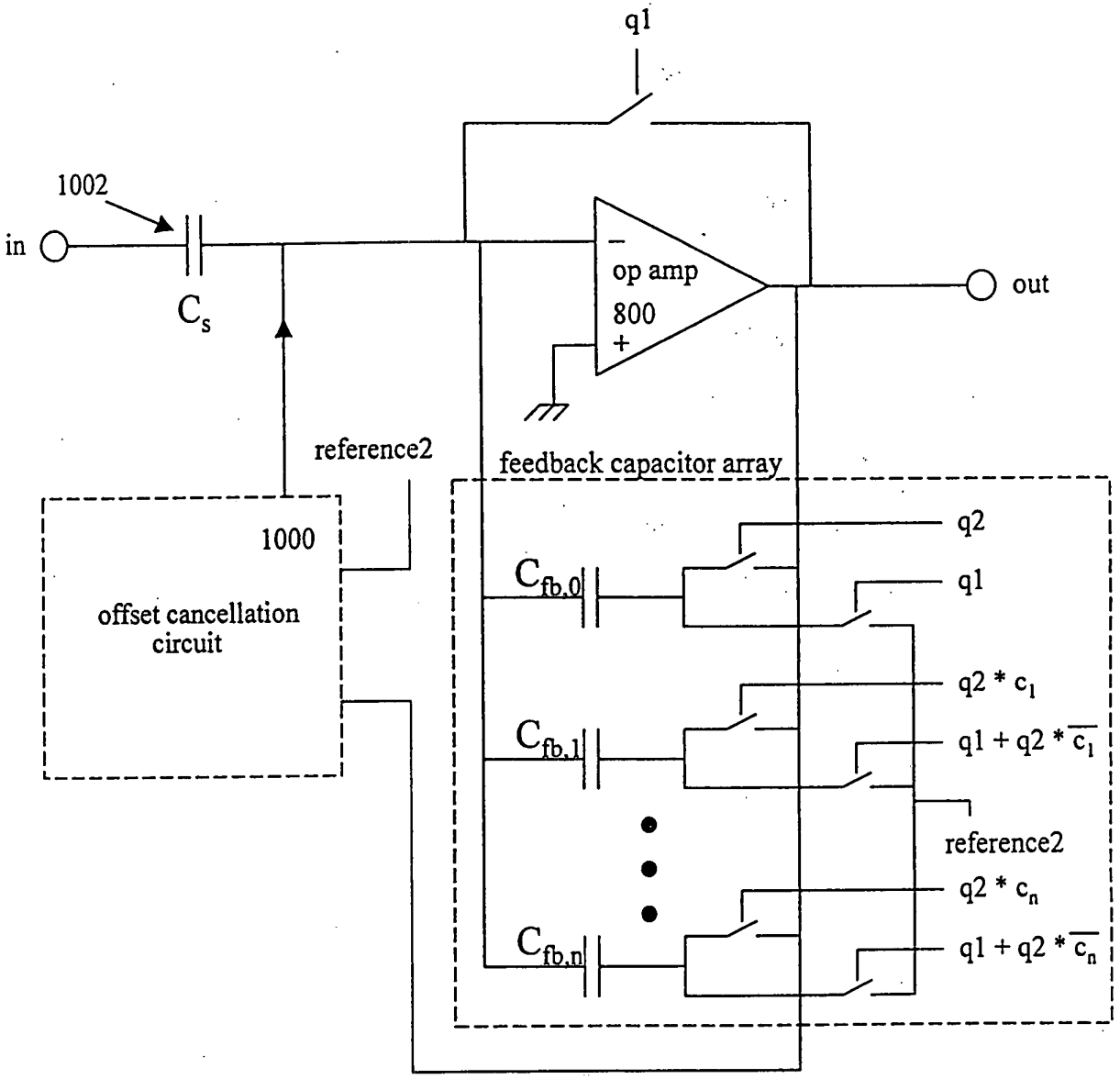

Figure 11: Implementation of Feedback Capacitor Array